M.TECH PROJECT LIST

1. AxPPA: Approximate Parallel Prefix Adders.
2. Adaptable Approximate Multiplier Design Based on Input Distribution and Polarity.
3. Efficient Design of Majority-Logic-Based Approximate Arithmetic Circuits.
4. BCD adder designs based on three-input XOR and majority gates.
5. High-speed area-efficient VLSI architecture of three-operand binary adder.
6. 64-bit ALU design using Vedic mathematics.
7. Single bit fault detecting ALU design using reversible gates.
8. A design implementation and comparative analysis of advanced encryption standard (AES) algorithm.
9. Modified high speed 32-bit Vedic multiplier design and implementation.
10. An implementation of high-speed adaptive recursive Karatsuba multiplier with square root-carry-select-adder.
11. Approximate Multiplier Design Using Novel Dual-Stage 4 : 2 Compressors.
12. Chaos-Based Bitwise Dynamical Pseudorandom Number Generator on FPGA.
13. TOSAM: An Energy-Efficient Truncation- and Rounding-Based Scalable Approximate Multiplier.
14. Design of logically obfuscated n-bit ALU for enhanced security.
15. Low-power high-accuracy approximate multiplier using approximate higher order compressors.
16. An Efficient Design of 16 Bit MAC Unit using Vedic Mathematics.
17. An implementation of multiplier-accumulator unit using Vedic multiplier and reversible gates.

18. Modified Dual-CLCG Method and Its VLSI Architecture for Pseudorandom Bit Generation.
19. A low-power yet high-speed configurable adder for approximate computing.
20. A low-power high-speed accuracy-controllable approximate multiplier design.
21. Towards Efficient Modular Adders based on Reversible Circuit.
22. MAES: Modified Advanced Encryption Standard for Resource Constraint Environments.
23. Chip design for turbo encoder module for in-vehicle system.
24. Design of Power and Area Efficient Approximate Multipliers.
25. Sustainable Fault Management and Error Correction for Next-Generation Main Memories.